Atty Dckt Number: 2102397-991220

PATENT

#7/B
2-12-03
L. Spruell

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

Chern et al.

Application No. 10/008,204

Filed: December 5, 2001

For: METHOD OF FORMING DIFFERENT OXIDE THICKNESS FOR HIGH VOLTAGE TRANSISTOR AND MEMORY CELL TUNNEL DIELECTRIC

Group Art Unit: 2826

Examiner: Pershelle L. Greene

RESPONSE TO OFFICE ACTION MAILED NOVEMBER 8, 2002

1755 Embarcadero Road
Palo Alto, CA 94303-3340
(650) 833-2000

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to Box Non-Fee Amendment, Assistant Commissioner for Patents, Washington, DC 20231, on January 27, 2003.

GRAY CARY WARE & FREIDENRICH Date: 1/27/03

By: Kathleen LaBrie

Kathleen LaBrie

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the Office Action mailed on November 8, 2002, please amend the above identified application as follows:

I. CLEAN VERSION OF CLAIMS AMENDED AND ADDED

A. Please substitute the following paragraph for the paragraph on page 7, lines 14-25 in this application:

In the memory cell area 32, a channel region 66 is defined in the substrate between the source 58 and drain 60. Poly layer 38 forms the cell's floating gate, which is disposed over and insulated from a first portion of the channel region 66 and a portion of the source region 58. Poly block 54 forms the cell's control gate, which includes a first portion 54a that is disposed over and insulated from a second portion of the channel region 66 and a portion of the drain 60, and is laterally adjacent to and insulated from the floating gate 38. The control gate 54 has a